SUMMARY OF THE INVENTION

The current invention provides a Fourier transform processor with a wide range of applications including communications, signal processing, medical and other imaging, seismic analysis, radar and other military applications, pattern recognition, signal processing etc.

The Fourier transform processor utilizes discrete circuits each of which is configurable for processing a wide range of sample sizes. A single pipeline supports multiplexed bi-directional transformations between for example the time and frequency domains. In an embodiment of the invention the Fourier Transform processor may be implemented as part of a digital signal processor (DSP) . In this embodiment the DSP may implement both the discrete Fourier transform (DFT) and inverse discrete Fourier transform (IDFT) across a wide range of sample sizes and X-DSL protocols. Multiple channels, each with varying ones of the X-DSL protocols can be handled in the same session.

In an embodiment of the invention a Fourier transform processor is disclosed. The processor includes: an input sample delivery circuit, at least one row and column circuit, and at least one sliced radix circuit. The input sample delivery circuit delivers a sample set of a one of N_f time domain samples and N_f frequency domain samples in a row and column order. The at least one row and column circuit performs a row and column transform on complex valued samples at the input to produce at the output coefficients corresponding with an other of the time domain and the frequency domain. The at least one sliced radix circuit of order "R" has R parallel inputs coupled to the input sample delivery circuit and an output coupled to the input of the at least one row and column circuit. The at least one sliced radix circuit transforms N_f /R input samples from the sample set into a selected one among the R possible complex outputs. The deliveries of the sample set to said at least one sliced radix circuit correspond in a number with the number of remaining ones among the R possible complex outputs.

In an alternate embodiment of the invention a method for computing a two dimensional Fourier transform is disclosed. The method comprising the acts of:

selecting a sample set of N_f samples corresponding with a one of a frequency domain and a time domain;

generating sliced radix transforms of an order R for each of N_f/ R selected subsets of the sample set, with each subset including R samples and with a slice corresponding

with a radix R transformation of the R inputs from each of the selected subsets to a selected one among R complex outputs;

completing row and column transforms on the complex outputs generated in said act of generating; and

repeating the generating and completing acts for each of a remaining ones of the R complex outputs, to transform the N_f samples of the sample set to the other of the frequency domain and the time domain.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features and advantages of the present invention will become more apparent to those skilled in the art from the following detailed description in conjunction with the appended drawings in which:

FIG. 1 depicts an overall system environment in which individual subscribers are coupled across public service telephone network (PSTN) subscriber lines with one or more high speed networks.

FIG. 2 depicts a more detailed view of a representative one of the central offices shown in FIG. 1 including both digital subscriber line access modules (DSLAMs) and PSTN voice band modules.

FIG. 3 is an expanded hardware view of one of the line cards in the central office shown in FIG. 2.

FIG. 4 is an expanded hardware view of the digital signal processor portion (DSP) of the line card shown in FIG. 3.

FIG. 5 shows the packet structure for passing data through and controlling the operation of various components within the DSP shown in FIG. 4.

FIG. 6 is a process flow diagram showing the operation of various shared and dedicated components within the DSP in response to the receipt of a upstream or downstream packet.

FIG. 7. is a data flow diagram showing the time required by Prior Art Fourier transform processors to process a sample.